REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-22 are pending in this application. Claims 1, 3, 8, 12, 14, and 19 are herein amended.

THE FINALITY OF THE OUTSTANDING OFFICE ACTION IS IMPROPER

Applicants submit the outstanding Office Action includes a new grounds for rejection that was ***not*** necessitated by any amendment on the part of the applicant, and thereby has prematurely been made a Final Rejection.

More specifically, the outstanding Office Action now rejects claims 3, 8, 14, and 19 under 35 U.S.C. § 112, second paragraph as the term "electrically connected" is not clear. Those claims 3, 8, 14, and 19 were ***not*** amended in the last response and those claims ***previously recited*** the phrase "electrically connected." The outstanding Office Action has now given a new rejection to those claims 3, 8, 14, and 19 for reciting the phrase "electrically connected" that was previously recited, and thus that rejection was ***not*** necessitated by any amendment on the part of the applicants.

Applicants submit setting forth such a new rejection in a Final Office Action is improper, and thereby the Finality of the Final Office Action must be withdrawn.

SUPPORT FOR CLAIM AMENDMENTS

Independent claims 1 and 12 now recite "at least every of first gates being formed in the gate forming region" and the CVD nitride film "not extending above an entire upper portion of the entire gate forming region in which said at least every first globe is formed". That subject matter is clear from the original specification, see for example Figure 2 showing

a plurality of gates 8 in a region and the CVD nitride film 14 not extending above any of those gates 8 in the region in which they are formed.

Each of claims 3, 14, and 19 is herein amended to recite the language "said first gate and said second gate are integrally formed and electrically connected to each other" and claim 8 is amended to recite the phrase "said first gate electrode and said second gate electrode are integrally formed and electrically connected to each other". Those amendments are believed to be clearly supported by the original disclosure, see for example Figure 4 .

ARGUMENTS

(1) Claims 1-22 were rejected under 35 U.S.C. § 112, second paragraph. (2) Claims 1-4, 7-9, 12-15, and 18-20 were rejected under 35 U.S.C. § 102(b) as anticipated by applicants' admitted art. (3) Claims 5, 6, 10, 11, 16, 17, 21, and 22 were rejected under 35 U.S.C. § 103(a) as unpatentable over the admitted art. Those rejections are traversed by the present response as now discussed.

(1) Rejection Under 35 U.S.C. § 112

Addressing now the rejection of claims 1-22 under 35 U.S.C. § 112, second paragraph, that rejection is traversed by the present response, as now discussed.

Claims 1 and 12 were rejected as reciting both "a gate forming region" and "a first gate region", and the relationship therebetween was unclear.

In reply to that rejection each of claims 1 and 12 is amended to no longer recite "a first gate region", but instead consistently recite "a gate forming region". The use of that consistent terminology is believed to address the above-noted grounds for the rejection.

Claims 1 and 12 were further rejected as the claim language directed to selectively forming the first semiconductor region of the second conductivity type in the first major surface of the first semiconductor layer was unclear, for example as to whether it was the

doping or the semiconductor layer itself that remains. The rejection also appears to indicate "only a portion of the first conductivity regions of the first semiconductor layer remains in the recited insular form and/or central portion".[1]

In reply to those grounds for rejection, applicants submit independent claims 1 and 12 are clear in that respect. Independent claims 1 and 12 clearly recite the "***first conductivity type*** first semiconductor layer remains" (emphasis added) at the noted peripheral portion and central portion. Applicants submit from that language it is clear that the doping state of that first conductivity region remains as the claims clearly set forth the first conductivity type first semiconductor layer remains. Thereby that subject matter is believed to be clear.

Applicants also submit that subject matter is clear from the original specification. Specifically, and with reference to Figures 2 and 3 in the present specification as a non-limiting example, in the claimed semiconductor device a first semiconductor layer 3 is formed, and then a first semiconductor region of a second conductivity type 11 is selectively formed in that first semiconductor layer 3. The formation of that second conductivity type first semiconductor region 11 results in the first semiconductor layer 3 of the first conductivity type no longer being present where the regions 11 are selectively formed, and thus at portions other than where that first semiconductor region of the second conductivity type 11 is formed the first semiconductor layer 3 will remain. Applicants submit such terminology is clear from the specification and Figures 2 and 3, and applicants submit such terminology is clearly understood by one of ordinary skill in the art.

Moreover, applicants note the claims already set forth the first semiconductor type first semiconductor layer remains along a peripheral portion and a central portion. That is, those claims already refer to the areas where the first conductivity type first semiconductor layer remains as ***portions***, and thereby applicants submit the claims are clear in that respect.

[1] Office Action of March 24, 2009, page 3, middle paragraph.

Stated another way, further amending claims 1 and 12 to recite that the first semiconductor type first semiconductor layer remains along "a portion of a peripheral portion" or "a portion of a central portion" does not appear to clarify the claims in any way, but only appears to make the claims grammatically awkward. Thereby, the claim language as currently written is believed to be proper.

In view of the foregoing comments applicants respectfully submit claims 1 and 12 are in full compliance with all requirements under 35 U.S.C. § 112, second paragraph.

Claims 3, 8, 14, and 19 were rejected as the term "electrically connected" was unclear. That noted language has been clarified in each of claims 3, 8, 14, and 19, to indicate the noted elements being "electrically connected to each other", which is believed to address the rejections thereto under 35 U.S.C. § 112, second paragraph.

In view of the foregoing comments, applicants respectfully submit each of claims 1-22 is proper under 35 U.S.C. § 112, second paragraph.

(2)-(3) Prior Art Rejections

Addressing now the above-noted prior art rejections over the admitted art, applicants respectfully submit the claims as currently written overcome that rejection.

Each of independent claims 1 and 12 as noted above is amended by the present response to clarify "at least every of first gates being formed in the gate forming region", and claims 1 and 12 additionally now recite the CVD nitride film does not extend above "an entire upper portion of the entire gate forming region in which said at least every first gate is formed". The claims thereby recite a structure that the CVD nitride film does not extend above an upper portion of any first gate in the claimed device, i.e. does not extend above an upper portion of any of the first gates 8.

The outstanding Office Action interpreted the admitted art to meet the claim limitations as in Figure 20 the layer 14 does not extend above the gate 8 underneath the

reference indicator 13. However, that gate 8 underneath the reference indicator 13 is only one gate. As clearly shown in Figure 20 in the present specification the CVD nitride film 14 extends above several of the gates 8 in a region of the gates.

Applicants respectfully submit the admitted art does not disclose or suggest the claimed features that an integral semi-insulating plasma CVD nitride film does not extend above an entire upper portion of an entire region of at least every of first gates. With reference to Figure 2 in the present specification as a non-limiting example, the semi-insulating plasma CVD film 14 as in the claimed invention does not extend above an upper portion of any of the first gates 8.

In maintaining the outstanding rejection, the outstanding Office Action states:

> Applicant's arguments appear to intend to imply that AAPA fails to show the feature of the instant invention that the integral semi-insulating plasma CVD nitride film does not extend above **any upper portion** of **any first gate or gates** in the claimed device. However, it is noted that such features upon which applicant relies are not recited in the rejected claim(s), which is especially true as the term of "an upper portion of the gate forming region" does not necessary have to be interpreted as meaning: the entire upper surface of the entire gate forming region.[2]

In reply to that grounds for rejection as noted above the claims are herein amended to recite the CVD nitride film does not extend above an entire upper surface of the entire first gate forming region.

Further, the applicants of the present invention recognized in the background art such as shown for example in Figures 19 and 20 in the present specification that a structure is known in which a protective film 14 would extend above different gates 8. The applicants of the present invention recognized drawbacks for such a system, discussed throughout the "Description of the Background Art" section of the present application.

[2] Office Action of March 24, 2009, middle of page 8 (original emphasis).

The applicants of the present invention in recognizing problems in the background art also recognized a solution to the problems, and particularly the solution being in limiting the extent of the CVD nitride film to not extend above an upper portion of a region in which all of first gates are formed. Without recognizing the problems in the background art pointed out in the specification, one of ordinary skill in the art would clearly not have been led to any solution of such problems, and particularly would not have been led to a solution that limits the extent of the CVD nitride film such as in the claims as written.

Moreover, the outstanding grounds for rejection is ignoring the fact that the admitted art does not even recognize any problems therein or any solution to such problems. The claimed invention recognized drawbacks in the admitted art and a specific solution of limiting the extent of a CVD nitride film to not extend above an upper portion of a region of all of first gates to solve such problems. Applicants submit such a structure is not disclosed in the admitted art and the admitted art does not achieve the benefits realized by the claimed structure.

Thereby, each of independent claims 1 and 12 as currently written is believed to positively recite a structure neither taught nor suggested by the admitted art of Figure 20. Thereby, each of claims 1-22 is believed to be allowable over the noted admitted art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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APPENDIX

Listing of Claims

1. (Currently Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

a first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first conductivity type first semiconductor layer remains along a peripheral portion of said first major surface, and said first conductivity type first semiconductor layer remains in a form of an insular region in a planar view in a central portion of said first major surface;

a second semiconductor region of the first conductivity type formed in a surface of said first semiconductor region, with a channel region provided between said second semiconductor region and said insular region of said first semiconductor layer;

a gate insulating film formed on a surface of said channel region;

a gate forming region formed on said gate insulating film, at least every of first [[gate]] gates being formed in ~~a first~~ the gate forming region;

an interlayer insulating film formed at least on said first gate:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said second semiconductor region and having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and

not extending above an entire upper portion of the entire gate forming region in which said at least every first gate is formed, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

2. (Original) The semiconductor device of claim 1, wherein

said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

3. (Currently Amended) The semiconductor device of claim 1, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected to each other.

4. (Original) The semiconductor device of claim 3, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

5. (Original) The semiconductor device of claim 4, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

6. (Original) The semiconductor device of claim 4, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

7. (Original) The semiconductor device of claim 1, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

8. (Currently Amended) The semiconductor device of claim 7, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate electrode and said second gate electrode are integrally formed and electrically connected to each other.

9. (Previously Presented) The semiconductor device of claim 8, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

10. (Original) The semiconductor device of claim 9, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

11. (Original) The semiconductor device of claim 9, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

12. (Currently Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

at least one first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first conductivity type first semiconductor remains along a peripheral portion of said first major surface, and said first conductivity type first semiconductor region remains in a form of a plurality of insular regions in a planar view in a central portion of said first major surface;

a plurality of second semiconductor regions of the first conductivity type formed in a surface of said at least one first semiconductor region, with channel regions provided between said second semiconductor regions and said insular regions of said first semiconductor layer;

a gate insulating film formed on a surface of said channel regions;

a gate forming region formed on said gate insulating film, at least every of first [[gate]] gates being formed in ~~a first~~ the gate forming region;

an interlayer insulating film formed at least on said first gate:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said plurality of second semiconductor regions, said first main electrode further having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film for covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending above an entire upper portion of the entire gate forming region in which said at least every first gate is formed, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

13. (Original) The semiconductor device of claim 12, wherein

said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

14. (Currently Amended) The semiconductor device of claim 13, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected to each other.

15. (Original) The semiconductor device of claim 14, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

16. (Original) The semiconductor device of claim 15, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

17. (Original) The semiconductor device of claim 15, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

18. (Original) The semiconductor device of claim 13, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

19. (Currently Amended) The semiconductor device of claim 18, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected to each other.

20. (Original) The semiconductor device of claim 19, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

21. (Original) The semiconductor device of claim 20, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10-10 (1/Ω cm).

22. (Original) The semiconductor device of claim 20, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} (1/Ω cm).